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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/673,262	09/30/2003	Keitaro Imai	243436US2SX	2071
22850	7590	03/10/2005	EXAMINER	
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C. 1940 DUKE STREET ALEXANDRIA, VA 22314			LINDSAY JR, WALTER LEE	
			ART UNIT	PAPER NUMBER
			2812	

DATE MAILED: 03/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/673,262

Applicant(s)

IMAI ET AL.

Examiner

Walter L. Lindsay, Jr.

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 14-20 is/are allowed.
- 6) ☒ Claim(s) 1-13 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>9/23/2003</u> . | 6) <input type="checkbox"/> Other: ____.  |

### **DETAILED ACTION**

This Office Action is in response to Application filed on 09/03/2003.

Currently, claims 1-20 are pending.

#### ***Information Disclosure Statement***

1. The information disclosure statement filed 11/18/2004 fails to comply with 37 CFR 1.98(a)(1), which requires the following: (1) a list of all patents, publications, applications, or other information submitted for consideration by the Office; (2) U.S. patents and U.S. patent application publications listed in a section separately from citations of other documents; (3) the application number of the application in which the information disclosure statement is being submitted on each page of the list; (4) a column that provides a blank space next to each document to be considered, for the examiner's initials; and (5) a heading that clearly indicates that the list is an information disclosure statement. The information disclosure statement has been placed in the application file, but the information referred to therein has not been considered.

#### ***Specification***

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

#### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148

USPQ 459 (1966), that are applied for establishing a background for determining

obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claim 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Ohnishi et al. (U.S. Patent No. 6,153,460 dated 11/28/2000) in view of Lee et al. (U.S.

Patent No. 6,838,369 filed 6/30/2003).

Ohnishi shows the method substantially as claimed in Figs. 2A-2F and corresponding text as: forming an underlying region (Fig 2a) including an interlevel insulating film (2) on a semiconductor substrate (1) (col. 7, lines 63-65); forming a film on the underlying region (6) (col. 7, line 66- col. 8, line 10); forming a hole in the film (col. 7, line 66-col. 8, line 10); filling the hole with a bottom electrode film (18) (col. 8, lines 11-14); forming a dielectric film (16) on the bottom electrode film (col. 8, lines 16-24); and forming a top electrode film (20) on the dielectric film (col. 8, lines 32-36) (claim 1). Ohnishi teaches that forming the dielectric film comprises: forming another film on the bottom electrode film; forming another hole reaching the bottom electrode film in said another film; and filling said another hole with the dielectric film (col. 8, lines 16-24) (claim 2). Ohnishi teaches the forming the underlying region comprises forming a plug

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(4) to be connected to the bottom electrode film in the interlevel insulating film (col. 7, lines 63-65) (claim 3). Ohnishi teaches that filling the hole is performed using a CMP process (col. 8, lines 11-14) (claim 4). Ohnishi shows the method substantially as claimed in Figs. 2A-2F and corresponding text as: forming an underlying region including an interlevel insulating film on a semiconductor substrate (col. 7, lines 63-65); forming a bottom electrode film (18) on the underlying region (col. 8, lines 11-14); forming a film (6) on the bottom electrode film (col. 7, line 66-col. 8, line 10); forming a hole reaching the bottom electrode film in the film (col. 7, line 66-col. 8, line 10); filling the hole with a dielectric film (col. 8, lines 25-31); and forming a top electrode film on the dielectric film (col. 8, lines 32-36) (claim 6). Ohnishi teaches the forming the underlying region comprises forming a plug (4) to be connected to the bottom electrode film in the interlevel insulating film (col. 7, lines 63-65) (claim 7). Ohnishi teaches that filling the hole is performed using a CMP process (col. 8, lines 11-14) (claim 8). Ohnishi shows the method substantially as claimed in Figs. 2A-2F and corresponding text as: forming an underlying region including an interlevel insulating film on a semiconductor substrate (col. 7, lines 63-65); forming a film on the underlying region (col. 7, line 66- col. 8, line 10); forming a hole in the alumina film (col. 7, line 66-col. 8, line 10); filling the hole with a conductive film to form a plug (col. 7, lines 63-65); forming a bottom electrode film on the plug (col. 7, line 66-col. 8, line 10); forming a dielectric film on the bottom electrode film (col. 8, lines 25-31); and forming a top electrode film on the dielectric film (col. 8, lines 32-36) (claim 10). Ohnishi teaches that forming the hole in the film comprises forming the hole in the film and the interlevel

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insulating film (col. 7, line 63-col. 8, line 10) (claim 11). Ohnishi teaches that filling the hole is performed using a CMP process (col. 8, lines 11-14) (claim 12).

Ohnishi lacks anticipation only in not explicitly teaching that: 1) the film is an alumina film (claims 1, 6 and 10); and 2) the dielectric film is a metal oxide film (claims 5, 9 and 13).

Lee teaches the use of an alumina film that is formed over an interlevel insulating film. The alumina film (108) is formed over a device (col. 3 lines 21-25). The alumina film is then etched to form a contact hole (114). This process is used to reduce the contact resistance of the cell that arises due to high integration (col. 1, lines 16-18).

It would be obvious to one of ordinary skill in the art, at the time the invention was made, to modify the method of Ohnishi to substitute alumina in the place of the film and that the dielectric film is a metal oxide film as taught by Lee with the motivation that Lee teaches that a reduction of contact resistance of the cell is achieved by using this process.

***Allowable Subject Matter***

1. Claims 1-20 are allowed.
2. The following is an examiner's statement of reasons for allowance: the prior art, either singly or in combination fails to anticipate or render obvious, the limitations of:

...covering upper and side surfaces of the bottom electrode film pattern with an alumina film;

removing a part of the alumina film to expose the upper surface of the bottom electrode film pattern and to leave a part of the alumina film, which is formed on the side surface of the bottom electrode film pattern;

forming a dielectric film on the exposed upper surface of the bottom electrode film pattern; and

forming a top electrode film on the dielectric film, as required by claim 14; and

...forming a dielectric film pattern on the bottom electrode film;

covering upper and side surfaces of the dielectric film pattern with an alumina film;

removing a part of the alumina film to expose the upper surface of the dielectric film pattern and to leave a part of the alumina film, which is formed on the side surface of the dielectric film pattern; and

forming a top electrode film on the exposed upper surface of the dielectric film pattern, as required by claim 18.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter L. Lindsay, Jr. whose telephone number is (571) 272-1674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Walter L. Lindsay, Jr.  
Examiner  
Art Unit 2812

WLL  
  
March 4, 2005